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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,483	10/02/2003	James P. Pequignot	BUR920020049US1	2482
24241	7590	07/12/2005	EXAMINER	
IBM MICROELECTRONICS INTELLECTUAL PROPERTY LAW 1000 RIVER STREET 972 E ESSEX JUNCTION, VT 05452			MANDALA, VICTOR A	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/605,483	Applicant(s) PEQUIGNOT ET AL.	
	Examiner Victor A. Mandala Jr.	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 May 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) 5-9 and 12-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 10 and 11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>2/15/04</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Election/Restrictions*

1. Claims 5-9 and 12-14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 5/11/05.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 10, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S.

Patent No. 6,399,990 Brennan et al.

2. Referring to claim 1, a triple well electrostatic discharge (ESD) network comprising: a substrate, (Figure 1 #2), of a first conductivity; an insulator region, (Figure 1 shown but not labeled), residing on the surface of the substrate, (Figure 1 #2); a first region of a second conductivity, (Figure 1 #6), being partially embedded in the insulator region and the substrate, (Figure 1 #2); a second region of the second conductivity, (Figure 1 #8), being completely embedded in the substrate, (Figure 1 #2), and partially embedded in the first region, (Figure 1 #6); a third region of the second conductivity, (Figure 1 #12), being partially embedded in the insulator region, the substrate, (Figure 1 #2), and the second region, (Figure 1 #8); a fourth region of the first conductivity, (Figure 1 #18), being embedded in the insulator region and being

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located between the first, (Figure 1 #6), and third regions, (Figure 1 #12); and an isolation region, (Figure 1 #10), forming a metallurgical junction between the fourth region, (Figure 1 #18), and the first, (Figure 1 #6), second, (Figure 1 #8), and third regions, (Figure 1 #12), for the conduction of electrostatic discharge.

3. Referring to claim 2, a triple well ESD network, wherein the isolation region, (Figure 1 #10), abuts the top surface of the second region, (Figure 1 #8), an edge of both of the second, (Figure 1 #8), and third regions, (Figure 1 #12), and the bottom of the fourth region, (Figure 1 #18).

4. Referring to claim 3, a triple well ESD network, wherein the first conductivity is p doped and the second conductivity is n doped, (Figure 1).

5. Referring to claim 4, a triple well ESD network, wherein the fourth region operates in the capacity of a cathode, and the first, second, and third regions operate in the capacity of an anode.

In reference to the claim language referring to [the function of the fourth region operates in the capacity of a cathode, and the first, second, and third regions operate in the capacity of an anode], intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

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6. Referring to claim 10, a semiconductor device comprising: a substrate, (Figure 1 #2); an insulator, (Figure 1 shown but not labeled), residing on top of the substrate, (Figure 1 #2); an n region, (Figure 1 #8), embedded in the substrate, (Figure 1 #2); a first n well, (Figure 1 #6), embedded in the insulator and bedded in the n region, (Figure 1 #8); a second n well, (Figure 1 #12), embedded in the insulator and partially embedded in the n region, (Figure 1 #8); a p region embedded, (Figure 1 #18), in the insulator between the first, (Figure 1 #6), and second n wells, (Figure 1 #12); an isolation region, (Figure 1 #10), forming a metallurgical junction between the p region, (Figure 1 #18), and the first n well, (Figure 1 #6), second n well, (Figure 1 #12), and n region, (Figure 1 #8), for the conduction of electrostatic discharge.

7. Referring to claim 11, a semiconductor device, wherein the p region operates in the capacity of an anode, and the first and second n wells, and n region operates in the capacity of a cathode.

In reference to the claim language referring to [the function of the p region operates in the capacity of an anode, and the first and second n wells, and n region operates in the capacity of a cathode], intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 10, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S.

Patent No. 6,891,207 Pequignot et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e).

This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

8. Referring to claim 1, a triple well electrostatic discharge (ESD) network comprising: a substrate, (Figure 1 #10), of a first conductivity; an insulator region, (Figure 1 #2 & 4), residing on the surface of the substrate, (Figure 1 #10); a first region of a second conductivity, (Figure 1 #3), being partially embedded in the insulator region, (Figure 1 #2 & 4), and the substrate, (Figure 1 #10); a second region of the second conductivity, (Figure 1 #8), being completely embedded in the substrate, (Figure 1 #10), and partially embedded in the first region, (Figure 1 #3); a third region of the second conductivity, (Figure 1 #3a), being partially embedded in the insulator region, (Figure 1 #2 & 4), the substrate, (Figure 1 #10), and the second region, (Figure

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1 #8); a fourth region of the first conductivity, (Figure 1 #5), being embedded in the insulator region, (Figure 1 #2 & 4), and being located between the first, (Figure 1 #3), and third regions, (Figure 1 #3a); and an isolation region, (Figure 1 #6), forming a metallurgical junction between the fourth region, (Figure 1 #5), and the first, (Figure 1 #3), second, (Figure 1 #8), and third regions, (Figure 1 #3a), for the conduction of electrostatic discharge.

9. Referring to claim 2, a triple well ESD network, wherein the isolation region, (Figure 1 #6), abuts the top surface of the second region, (Figure 1 #8), an edge of both of the second, (Figure 1 #8), and third regions, (Figure 1 #3a), and the bottom of the fourth region, (Figure 1 #5).

10. Referring to claim 3, a triple well ESD network, wherein the first conductivity is p doped and the second conductivity is n doped, (Figure 1).

11. Referring to claim 4, a triple well ESD network, wherein the fourth region operates in the capacity of a cathode, and the first, second, and third regions operate in the capacity of an anode. In reference to the claim language referring to [the function of the fourth region operates in the capacity of a cathode, and the first, second, and third regions operate in the capacity of an anode], intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

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12. Referring to claim 10, a semiconductor device comprising: a substrate, (Figure 1 #10); an insulator, (Figure 1 #2 & 4), residing on top of the substrate, (Figure 1 #10); an n region embedded, (Figure 1 #8), in the substrate, (Figure 1 #10); a first n well, (Figure 1 #3), embedded in the insulator, (Figure 1 #2 & 4), and bedded in the n region, (Figure 1 #8); a second n well, (Figure 1 #3a), embedded in the insulator, (Figure 1 #2 & 4), and partially embedded in the n region, (Figure 1 #8); a p region, (Figure 1 #5), embedded in the insulator, (Figure 1 #2 & 4), between the first, (Figure 1 #3), and second n wells, (Figure 1 #3a); an isolation region, (Figure 1 #6), forming a metallurgical junction between the p region, (Figure 1 #5), and the first n well, (Figure 1 #3), second n well, (Figure 1 #3a), and n region, (Figure 1 #8), for the conduction of electrostatic discharge.

13. Referring to claim 11, a semiconductor device, wherein the p region operates in the capacity of an anode, (Col. 3 Lines 62-63), and the first and second n wells, and n region operates in the capacity of a cathode, (Col. 4 Lines 1-2).

### ***Conclusion***

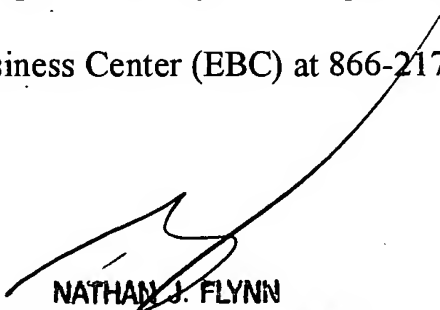
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ  
7/7/05



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